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SpikeFun - Cortical Neural Network Simulator

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In order to perform system performance testing, SpikeBenchmark is using DigiCortex engine which is simulating mammalian cortex (to be more precise: thalamocortical system). Neuron modeling is phenomenological and biophysically accurate to the level of spike responses.

As large-scale biological simulation such as this is extremely CPU and even more so memory intensive, SpikeBenchmark can be used as a good tool for system performance measurement, especially regarding memory bandwidth and, to some extent, CPU floating point calculation performance.

There are 4 default benchmarks offered by SpikeBenchmark:

- [1] Small-scale simulation (32768 neurons, ~1.8 million synapses): recommended for benchmarking desktop PCs
- [2] Small-scale simulation benchmark (same as 1) with maximum memory bandwidth tested (basically running the simulation in 'silent' state with no active neurons): recommended for benchmarking of the memory subsystem of the desktop PC
- [3] Large-scale simulation benchmark (262144 neurons, ~37 million synapses): recommended for benchmarking servers/workstations. Please note: this preset requires at least 6 GB of RAM
- [4] Large-scale simulation benchmark (same as 3) with maximum memory bandwidth tested (basically running the simulation in 'silent' state with no active neurons): recommended for benchmarking of the memory subsystem of the server/workstation system. Please note: this preset requires at least 6 GB of RAM

SpikeBenchmark is also able to measure and log consumed memory bandwidth on Intel(r) Sandy Bridge EP ('Jaketown') CPUs. During the benchmark, CPU power draw as well as IPC rate will be logged on supported Intel(r) CPUs, using hardware performance monitoring unit (PMU).

Please note that for hardware counter collection, following

requirements apply:

- Supported CPUs: Intel CPUs with the micro-architecture codenames 'Nehalem', 'Nehalem EP', 'Nehalem Ex', 'Westmere', 'Westmere EP', 'Westmere EX', 'Clarkdale', 'Sandy Bridge' and 'Sandy Bridge EP - Jaketown'
- CPU power readouts are supported on Intel CPUs with microarchitecture codenames 'Sandy Bridge' and 'Sandy Bridge EN/EP - Jaketown' (e.g. second generation Core i7 and second generation Core i7 Extreme, Intel Xeon E5 1600/2600/4600)

Memory bandwidth readouts are supported on Intel CPUs with micro-architecture codenames: 'Nehalem', 'Nehalem EP', 'Nehalem EX', 'Westmere', 'Westmere EP', 'Westmere EX' and Sandy Bridge EN/EP - Jaketown (e.g. Socket 1366 and Socket 2011 based Intel Core i7 and Xeon 5500 / E5 1600/2600/4600 CPUs)

Please note: reading of PMU registers require loading and using ofring0 driver WinRing0.sys or (or WinRing0x64.sys). This typically requires running of the benchmark with administrator privileges.

WinRing0 driver is Copyright © 2007-2009 OpenLibSys.org, please see WinRing0.License.txt for details.

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SpikeBenchmark PMU counter access is implemented by using Intel's Performance Counter Monitor (PCM) library, which is available for download in source code form from the following link:

<http://software.intel.com/en-us/articles/intel-performance-counter-monitor/>

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